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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,791	09/08/2003	Kia Silverbrook	BAL52US	8951

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SILVERBROOK RESEARCH PTY LTD
393 DARLING STREET
BALMAIN, 2041
AUSTRALIA

EXAMINER	
MENBERU, BENIYAM	

ART UNIT	PAPER NUMBER
2625	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/656,791	SILVERBROOK, KIA	
	Examiner	Art Unit	
	BENIYAM MENBERU	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/20/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 6, 2008 has been entered.

Response to Arguments

2. Applicant's arguments with respect to claim 1 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 120 as follows:

The later-filed application must be an application for a patent for an invention which is also disclosed in the prior application (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the

requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

The disclosure of the prior-filed application, Application No. 09/113053, fails to provide adequate support or enablement in the manner provided by the first paragraph of 35 U.S.C. 112 for one or more claims of this application.

The current application 10/656791 claims a **one-chip microcontroller integrating** on the one chip a VLIW processor, image sensor interface, and a printhead interface.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 8 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 8 discloses the "VLIW processor running the program from the memory device" which is not disclosed in the original specification

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 3, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al in view of U.S. Patent No. 5875034 to Shintani et al.

Regarding claim 1, Petit et al '310 discloses an image sensing digital camera device (see Abstract) comprising:

a housing (Figure 1, dashed lines show camera housing) ;

an area image sensor positioned on the housing for sensing a viewed image (Figure 1, CMOS image sensor; Introduction second paragraph) for generating pixel data representing the viewed image (see Introduction, seventh paragraph);

a one-chip microcontroller that is positioned in the housing (Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph), the one-chip microcontroller integrating on the one chip a VLIW processor (Figure 1, shows VLIW processor integrated on the one-chip; Introduction sixth paragraph), an image sensor interface connected to the VLIW processor for receiving pixel data from the image sensor (Figure 1, shows interface between CMOS sensor and ADC (analog to digital converter); Introduction seventh paragraph), converting the pixel data into an internal format and

writing the converted pixel data to the processing circuitry (Introduction: seventh and eighth paragraph; ADC converts to digital format for writing into register; converted data can be outputted to bus interface as shown in Figure 1). Petit et al '310 does not expressly disclose a print interface for printing sensed image data wherein the processing circuitry being configured to convert the pixel data to print image data.

However, it is well known in the art to transfer image data for printing using the IEEE 1934 interface shown in Petit et al '310 in Figure 1.

Thus this interface can provide a printing interface and the processing circuitry configured to convert the pixel data to print image data for the one-chip disclosed in Petit et al '310.

It would have been obvious at the time the invention was made to one of ordinary skill in the art to provide Petit et al '310, with the well known ability to provide a printing interface.

However Petit et al '310 does not disclose:

printing digital camera device;

an area image sensor positioned on the housing for sensing a viewed image to be printed on media;

a printing mechanism that is arranged on the housing;

a printhead interface connected to the processor for receiving the print image data from the processor and for providing signals representing the print image data to the printhead so that the printhead can carry out said printing operation to generate a printed representation of said viewed image.

Shintani et al '034 discloses:

printing digital camera device (Figure 1, CCD 101; column 7, lines 23-30; Figure 1, reference 111; column 7, lines 60-66);

an area image sensor positioned on the housing for sensing a viewed image to be printed on media (column 7, lines 24-30; CCD is sensor; column 10, lines 9-44; memory 311, 312 store image data from sensor ; RGB image data; column 20, lines 8-19; pixel; column 12, lines 63-67; column 13, lines 1-15; images in memory 311, 312 is printed on media (column 14, lines 13-16; recording sheet).);

a printing mechanism that is arranged on the housing (column 6, lines 21-25; printer case; Figure 1 reference 111 is printer (column 7, lines 12-21;);

a printhead interface connected to the processor for receiving the print image data from the processor and for providing signals representing the print image data to the printhead so that the printhead can carry out said printing operation to generate a printed representation of said viewed image (Figure 1 shows interface between processor 102 and printer 111; Figure 5 shows print head unit 400, 403, 410; column 13, lines 63-67; column 14, lines 1-6;).

Having the system of ***Petit et al '310*** and then given the well-established teaching of ***Shintani et al '034***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310*** as taught by ***Shintani et al '034***, since ***Shintani et al '034*** stated in col. 3, Lines 55-67; column 4, lines 1-2, such a modification would provide a camera with embedded printer for providing user specified mode of printing.

Regarding claim 2, Petit et al '310 in view of Shintani et al '034 teaches all the limitations of claim 1. Further Shintani et al '034 discloses a device as claimed in claim 1, in which the area image sensor is one of a charge coupled device and an active pixel sensor (Figure 1, CCD 101; column 7, lines 23-30).

Regarding claim 3, Petit et al '310 in view of Shintani et al '034 teaches all the limitations of claim 1. Further Shintani et al '034 discloses a device as claimed in claim 1, in which the printing mechanism includes an ink distribution assembly that is mounted on the print head assembly to distribute ink to the print head chips (column 18, lines 1-9, head 410 is pressed onto ink ribbon).

Regarding claim 5, Petit et al '310 in view of Shintani et al '034 teaches all the limitations of claim 1. Further Petit et al '310 in view of Shintani et al '034 discloses a device as claimed in claim 1, in which the one-chip microcontroller (Petit et al '310: Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph) is configured to be programmable with any of a number of image processing programs so that the one-chip microcontroller can carry out image processing operations on the pixel data in accordance with a selected program loaded on the one-chip microcontroller (Shintani et al '034: column 12, lines 34-42, 63-67; column 13, lines 1-5, 16-20; tv mode, printing mode, and multi-image are the image processing programs that are executed depending on the mode).

Regarding claim 6, Petit et al '310 in view of Shintani et al '034 teaches all the limitations of claim 5. Further Petit et al '310 discloses a **one-chip microcontroller** (Petit et al '310: Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph) and Shintani et al '034 discloses a device as claimed in claim 5, which includes a reader for reading said any of a number of image processing programs stored on a data storage device and a reader interface for writing the program to the **controller** (Shintani et al '034: column 12, lines 11-19 (information read from memory card); column 12, lines 34-42, 63-67; column 13, lines 1-5, 16-20; processor 100 is programmed to perform processing depending on the mode. When the processor 100 is programmed to execute processing (column 13, lines 16-20), that reads on writing program to the processor.).

8. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over XP-002353310, "VLIW Processor Architecture Adapted to FPAs" to Petit et al in view of U.S. Patent No. 5875034 to Shintani et al further in view of U.S. Patent Application Publication No. US 2002/0024603 A1 to Nakayama et al.

Regarding claim 7, Shintani et al '034 in view of Bagchi et al '358 teach all the limitations of claim 6. Petit et al '310 discloses a one-chip microcontroller (Petit et al '310: Figure 1, shows one-chip microcontroller; see Abstract; Introduction first paragraph). However Shintani et al '034 in view of Bagchi et al '358 does not disclose a device as claimed in claim 6, in which the reader is an optical reader for reading a two-dimensional pattern printed on a planar element, the two-dimensional pattern

representing a program in an image processing language, the optical reader being configured to generate program data and the reader interface being configured to receive the program data and to write the program data, in an internal format, to the microcontroller.

Nakayama et al disclose a device as claimed in claim 6, in which the reader is an optical reader for reading a two-dimensional pattern printed on a planar element, the two-dimensional pattern representing a program in an image processing language, the optical reader being configured to generate program data and the reader interface being configured to receive the program data and to write the program data, in an internal format, to the microcontroller (page 3, paragraph 54; page 2, paragraph 32,33,34).

Having the system of ***Petit et al '310 in view of Shintani et al '034*** and then given the well-established teaching of ***Nakayama et al '603***, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the system of ***Petit et al '310 in view of Shintani et al '034*** as taught by ***Nakayama et al '603***, since ***Nakayama et al '603*** stated in page 1, paragraph 17, such a modification would provide alternate method for controlling the image device by loading the program from external source.

Regarding claim 8, Petit et al '310 in view of Shintani et al '034 further in view of Nakayama et al '603 teaches all the limitations of claim 7. Further Petit et al '310 discloses a device in which the one-chip microcontroller includes a memory device (Figure 1, the one-chip has instruction and data memory), the VLIW processor being configured to write the program data in the internal format to the memory device (page

129, fourth paragraph; instructions are stored in instruction memory), and Shintani et al '034 disclose the processor running the program from the memory device to define a software algorithm by which registers in the printhead interface are addressed to apply a desired effect to the print image data (processor 100 is programmed to execute processing (column 13, lines 16-20); Figure 1, processor 100 interfaces the printing section 111; column 13, lines 1-15; "desired print system" on column 13, line 11; column 13, lines 16-20, 56-61; One desired effect is multi-image effect which can print multi-image. Column 19, lines 9-25; head unit contains registers 501, 502).

Other Prior Art Cited

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Application Publication No. US2001/0051766 A1 to Gazdzinski discloses device having VLIW processor.

U.S. Patent No. 5757432 to Dulong et al disclose a computer.

Fujioka et al, "Reconfigurable parallel VLSI processor for dynamic control of intelligent robots", January 1996, IEE Proc.-Comput. Digit. Tech., Vol. 143, No. 1, pp. 23-29.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENIYAM MENBERU whose telephone number is (571) 272-7465. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Moore can be reached on (571) 272-7437. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the customer service office whose telephone number is (571) 272-2600. The group receptionist number for TC 2600 is (571) 272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov/>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Beniyam Menberu

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Examiner, Art Unit 2625

12/5/2008

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